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EDITORIAL INTRODUCTION

Special Issue on Networks-on-Chips: Design Flows and Case Studies

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We are pleased to present this special issue of the Journal of Design Automation for Embedded Systems entitled: **Networks-on-chips: Design Flows and Case Studies**.

Networks-on-chips (NoCs) have been an active field of research for a number of years, and NoCs have already become the mainstream technology for many applications. Thus it is important to expand the research and practice of NoCs beyond their hardware and software architectures. The four papers selected for this special issue aim precisely at this by addressing topics related to voltage-frequency islands (VFI) partitioning and self-recovering NoCs, a commercial design flow for NoCs, and the cost-performance trade offs of NoCs in a large case study.

The first paper is entitled *Communication-Aware VFI Partitioning for GALS-based Networks-on-Chip*, by Dongkun Shin, Woojoong Kim, Soontae Kwon, and Tae Hee Han, of the Sungkyunkwan University in Korea, discusses the important issue of determining the voltage-frequency domains in commonly-used globally asynchronous local synchronous (GALS) SoC design styles, by taking communication requirements into account, while minimising area and energy.

The second paper, by Kun-Chih Chen, Shu-Yen Lin, Wen-Chung Shen, and An-Yeu (Andy) Wu, of the National Taiwan University in Taiwan, titled *A Scalable Built-In Self-Recovery (BISR) VLSI Architecture and Design Methodology for 2D-Mesh Based On-Chip Networks*, proposes ways to make future NoCs more robust to faults, via fault detection and diagnosis, and self-recovery.

The third paper, *Application Driven Network-on-Chip Architecture Exploration & Refinement for a Complex SoC*, is an industrial contribution by Jean-Jacques Lecler and Gilles

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Baillieu of Arteris, one of the commercial providers of NoCs. The authors provide good insights into how NoCs can be generated for real SoC designs using Arteris's state-of-the-art industrial work flow.

The final paper, *A Quantitative Evaluation of a Network-on-Chip Design Flow for Multi-Core Consumer Multimedia Applications*, is by Andreas Hansson and Kees Goossens, from Arm Ltd. and Eindhoven University of Technology, respectively. The authors evaluate the Aethereal NoC in two large-scale industrial case studies from the digital TV and automotive radio domains, with different characteristics.

We hope readers will enjoy and benefit from reading these four papers that position NoCs as essential components within the larger system context.